In the Claims:

Please cancel claims 1-2, 4, 6-11, 15, 17, 23-25, and 27. Please amend claims 3, 5-6, 12-14, 16, 18-22, and 28-33. Please add new claims 34-XX. The claims are as follows:

1-2. (Canceled)

3. (Currently amended) The model of claim 12, wherein the model is implemented in the VHDL hardware description language using Vital timing routines.

4. (Canceled)

5. (Currently amended) The model of claim [[4]] 12, wherein the control mechanism enables the first path by enabling the second NMOS device when a change is detected on the first port and the first port does not equal the second port, and wherein the control mechanism enables the second path by enabling the first NMOS device when a change is detected on the second port and the first port does not equal the second port.

6-11. (Canceled)

12. (Currently amended) A model for representing a bidirectional wire input/output (I/O) during computer simulation of an electronic device, the model being tangibly embodied in a computer readable memory unit that comprises a Hardware Description Language (HDL) application program therein, the model being adapted to be used in a computer simulation of the electronic device by executing the HDL application program on a processor of a computer system, the model comprising:

a) a first path between a first port and a second port, the first path including a second NMOS device,

b) a second path between the second port and the first port, the second path including a first NMOS device; and

c) a control mechanism, the control mechanism checking signal values (S1) on the first port and signal values (S2) on the second port when a change is detected on the first port or the second port, the control mechanism enabling the second NMOS device when a change is detected on the first port and the first port does not equal the second port, the control mechanism enabling the first NMOS device when a change is detected on the second port and the first port does not equal the second port, wherein the second path further includes a third NMOS device and wherein the first path further includes a fourth NMOS device, wherein the third and fourth NMOS devices are tied on to function as pass devices.

13. (Currently amended) The model of claim 12, wherein the timing values are annotated into

the model in the form of module input port delays annotated into the third NMOS device and the fourth NMOS device.

14. (Currently amended) The model of claim ~~11~~ 12, wherein the timing values are annotated into the model in the form of propagation delays across the first path and the second path.

15. (Canceled)

16. (Currently amended) The model of claim ~~11~~ 12, wherein the control mechanism further disables the first NMOS device when a change is detected on the first port and the first port does not equal the second port, and wherein the control mechanism further disables second NMOS device when a change is detected on the second port and the first port does not equal the second port.

17. (Canceled)

18. (Currently amended) The method of claim ~~17~~ 20, further comprising the steps of:

e) disabling the second path when a change is detected on the first port and the first port does not equal the second port;

f) disabling the first path when a change is detected on the second port and the first port does not equal the second port.

19. (Currently amended) The method of claim ~~17~~ 20, further comprising the step of annotating timing values across the first path and the second path.

20. (Currently amended) ~~The method of claim 17~~ A method for representing a bidirectional wire input/output (I/O) during a computer simulation of an electronic device, the method comprising:

a) providing a model for the bidirectional wire I/O, the model including:

i) a first path between a first port and a second port; and

ii) a second path between the second port and the first port;

b) checking signal values (S1) on the first port and signal values (S2) on the second port when a change is detected on the first port or the second port;

c) enabling the first path when a change is detected on the first port and the first port does not equal the second port;

d) enabling the second path when a change is detected on the second port and the first port does not equal the second port, wherein the model further includes ~~a wherein~~ a second NMOS device and a fourth NMOS device in the first path and further includes a first NMOS device and a third NMOS device in the second path.

21. (Currently amended) The method of claim 20, further comprising the step of annotating module input port delays into the third NMOS device and the fourth NMOS device.

22. (Currently amended) A program product comprising:

A) a hardware description language model for representing a bidirectional wire input/output (I/O) during a computer simulation of a electronic device, the hardware description language model including:

i) a first path between a first port and a second port;

ii) a second path between the second port and the first port; and

iii) a control mechanism, the control mechanism checking signal values (S1) on the first port and signal values (S2) on the second port when a change is detected on the first port or the second port, the control mechanism enabling the first path when a change is detected on the first port and the first port does not equal the second port, the control mechanism enabling the second path when a change is detected on the second port and the first port does not equal the second port;

B) ~~signal-bearing~~ recordable media bearing the hardware description language model, wherein the first path comprises a second NMOS device and a fourth NMOS device, and wherein the second path comprises a first NMOS device and a third NMOS device.

23-25. (Canceled)

26. (Currently amended) The program product of claim 22, wherein the model is implemented in the VHDL hardware description language using Vital timing routines.

27. (Canceled)

28. (Currently amended) The program product of claim ~~27~~ 22, wherein the control mechanism enables the first path by enabling the second NMOS device when a change is detected on the first port and the first port does not equal the second port, and wherein the control mechanism enables the second path by enabling the first NMOS device when a change is detected on the second port and the first port does not equal the second port.

29. (Currently amended) The program product of claim ~~27~~ 22, wherein the first NMOS device, the second NMOS device, the third NMOS device, and the fourth NMOS device comprise Verilog NMOS primitives.

30. (Currently amended) The program product of claim ~~27~~ 22, wherein timing values are annotated into the model that include module input port delays annotated into the third NMOS device and the fourth NMOS device.

31. (Currently amended) The program product of claim ~~27~~ 22, wherein timing values are annotated across the first path and the second path.

32. (Currently amended) The program product of claim 31, wherein the timing values are annotated in the form of propagation delays annotated between the first port to the second

port and between the second port to the first port.

33. (Currently amended) The program product of claim 22, wherein the control mechanism further disables the second path when a change is detected on the first port and the first port does not equal the second port, and wherein the control mechanism further disables the first path when a change is detected on the second port and the first port does not equal the second port.

34. (New) The model of claim 12, wherein the first path and the second path are electrically in parallel, wherein the second NMOS device and the fourth NMOS device are electrically in series within the first path, wherein the first NMOS device and the third NMOS device are electrically in series within the second path.

35. (New) The model of claim 34, wherein the control mechanism uses HDL register values to detect the change on both the first port and the second port.

36. (New) The model of claim 34, wherein the gates of the third and fourth NMOS devices are held high throughout the computer simulation of the electronic device.

37. (New) The model of claim 36, wherein the control mechanism comprises a first control output C1 directly coupled to the gate of the first NMOS device and a second control

output C2 directly coupled to the gate of the second NMOS device, wherein the signal values (S1) at the first port are directly coupled to a source/drain of the first NMOS device, and wherein the signal values (S2) at the second port are directly coupled to a source/drain of the second NMOS device.

38. (New) The model of claim 37, wherein a state of an NMOS device selected from the group consisting of the first NMOS device and the second NMOS device is dictated by the following truth table, wherein if the NMOS device is the first NMOS device then S denotes the signal values S1 and C denotes the control output C1, and wherein if the NMOS device is the second NMOS device then S denotes the signal values S2 and C denotes the control output C2, wherein L denotes low, H denotes high, Z denotes high impedance, and X denotes undetermined:

		C			
		0	1	X	Z
S	0	Z	0	L	L
	1	Z	1	H	H
	X	Z	X	X	X
	Z	Z	Z	Z	Z

39. (New) The model of claim 20, wherein the first path and the second path are electrically in parallel, wherein the second NMOS device and the fourth NMOS device are electrically in series within the first path, wherein the first NMOS device and the third

NMOS device are electrically in series within the second path.

40. (New) The model of claim 39, wherein the control mechanism uses Hardware Description Language (HDL) register values to detect the change on both the first port and the second port.

41. (New) The model of claim 39, wherein the gates of the third and fourth NMOS devices are held high throughout the computer simulation of the electronic device.

42. (New) The model of claim 41, wherein the control mechanism comprises a first control output C1 directly coupled to the gate of the first NMOS device and a second control output C2 directly coupled to the gate of the second NMOS device, wherein the signal values (S1) at the first port are directly coupled to a source/drain of the first NMOS device, and wherein the signal values (S2) at the second port are directly coupled to a source/drain of the second NMOS device.

43. (New) The model of claim 42, wherein a state of an NMOS device selected from the group consisting of the first NMOS device and the second NMOS device is dictated by the following truth table, wherein if the NMOS device is the first NMOS device then S denotes the signal values S1 and C denotes the control output C1, and wherein if the NMOS device is the second NMOS device then S denotes the signal values S2 and C

denotes the control output C2, wherein L denotes low, H denotes high, Z denotes high impedance, and X denotes undetermined:

		C			
		0	1	X	Z
S	0	Z	0	L	L
	1	Z	1	H	H
	X	Z	X	X	X
	Z	Z	Z	Z	Z

44. (New) The model of claim 22, wherein the first path and the second path are electrically in parallel, wherein the second NMOS device and the fourth NMOS device are electrically in series within the first path, wherein the first NMOS device and the third NMOS device are electrically in series within the second path.

45. (New) The model of claim 44, wherein the control mechanism uses Hardware Description Language (HDL) register values to detect the change on both the first port and the second port.

46. (New) The model of claim 44, wherein the gates of the third and fourth NMOS devices are held high throughout the computer simulation of the electronic device.

47. (New) The model of claim 46, wherein the control mechanism comprises a first control

output C1 directly coupled to the gate of the first NMOS device and a second control output C2 directly coupled to the gate of the second NMOS device, wherein the signal values (S1) at the first port are directly coupled to a source/drain of the first NMOS device, and wherein the signal values (S2) at the second port are directly coupled to a source/drain of the second NMOS device.

48. (New) The model of claim 47, wherein a state of an NMOS device selected from the group consisting of the first NMOS device and the second NMOS device is dictated by the following truth table, wherein if the NMOS device is the first NMOS device then S denotes the signal values S1 and C denotes the control output C1, and wherein if the NMOS device is the second NMOS device then S denotes the signal values S2 and C denotes the control output C2, wherein L denotes low, H denotes high, Z denotes high impedance, and X denotes undetermined:

		C			
		0	1	X	Z
S	0	Z	0	L	L
	1	Z	1	H	H
	X	Z	X	X	X
	Z	Z	Z	Z	Z